CoEPP

ARC Centre of Excellence for Particle Physics at the Terascale

DAQ detector development in Adelaide for ATLAS upgrade

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R & D program's goals and phases

- *DAQ/trigger "technology"* for next generation HEP experiments…
  - One component of ongoing Detector R & D project (driven by SLAC)
- "Phase 0"
  - "Survey the requirements and capture their commonality"
  - Intended to leverage recent industry innovation
  - Project's cultural bias, "one size does not fit all". Leads to…
  - The concept of ubiquitous building blocks
    - The (*Reconfigurable) Cluster Element* (RCE)
    - The *Cluster Interconnect* (CI)
    - Industry standard packaging (*ATCA*)
- "Phase 1"
  - Technology evaluation & demonstration hardware
    - The RCE & CI boards
- "Phase 2"
  - Useful, sustainable architecture (how to future proof)
    - Generic ATCA Front-Board (the COB) & the RCE "GEN-II"
- "Phase 3"
  - Meet all RCE related performance goals
    - Move to ASP (ARM based silicon)

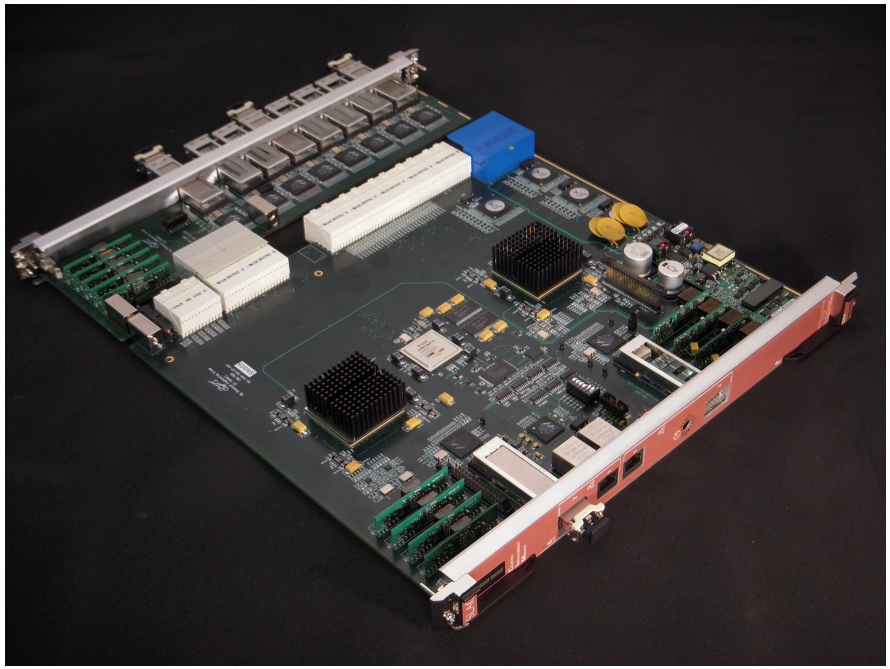
In Adelaide we're using Gen I hardware with Gen II setup

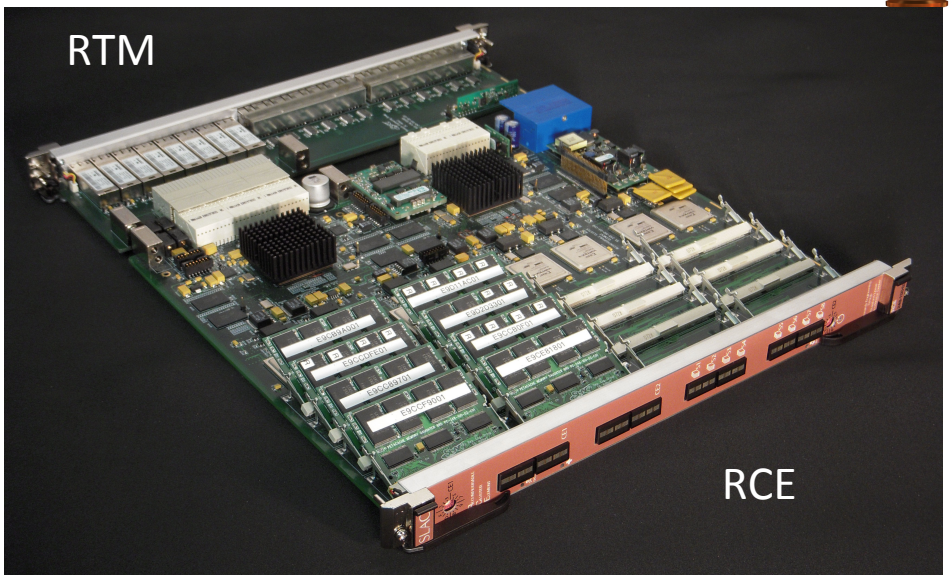
This is where the current R&D program is

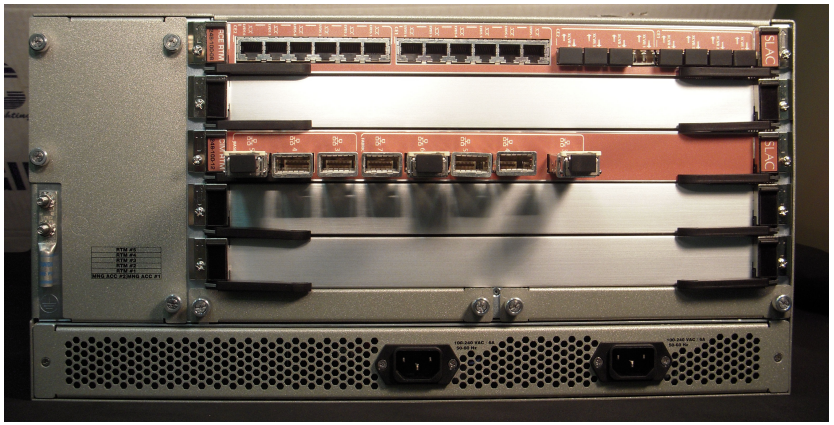
RCE uses in ATLAS

- Where RCE related DAQ has been applied in ATLAS
- ATLAS upgrade related activities
  - IBL – (insertable b-layer) Read/Out (R/O)
  - CSC ROD replacement
  - Full pixel R/O system replacement for phase II upgrade
  - Forward Muon Readout (small wheel replacement)
  - Case studies on alternative architectures
    - Integration of ROD + ROS functionality
    - Level 1.5 triggers (integrated to FTK (Fast TracK Trigger)?
    - +others ??

Gen I RCE board and RTM – Some elements of the Adelaide setup







These are combined in the ATCA crate

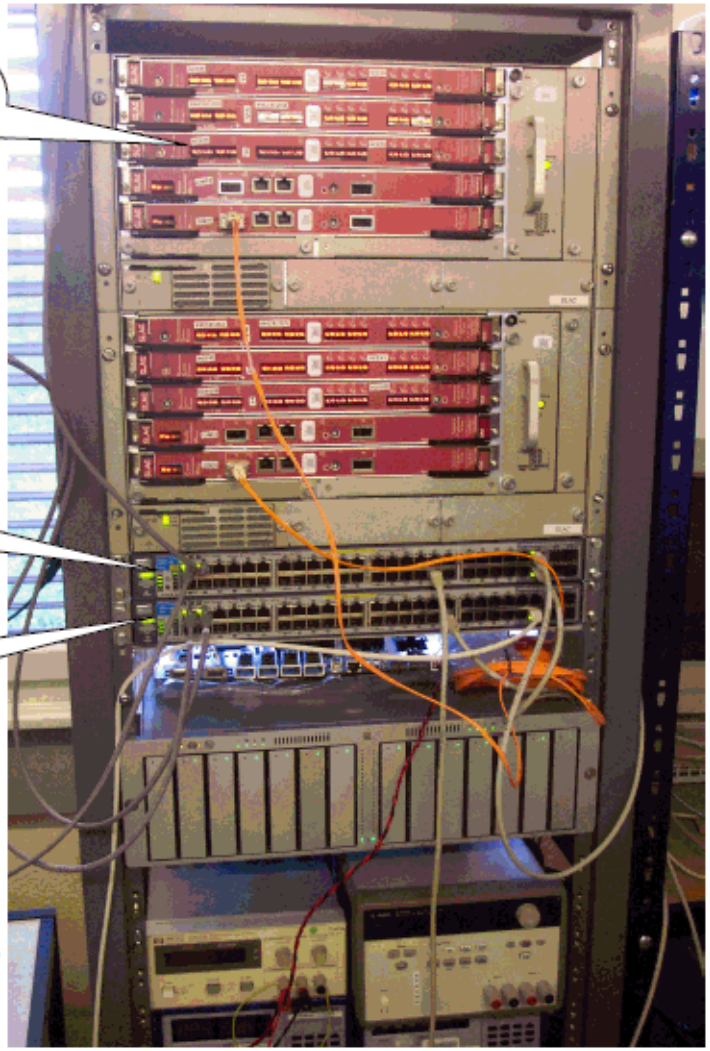
Test stand for DAQ @ CERN

Installation in Bldg 32

RCE/CIM
ATCA Crates

DAQ Switch
48x1GE + 2x10GE

GPN Switch
48x1GE



HP ProCurve 3500yl
2x 10GE X2 SR

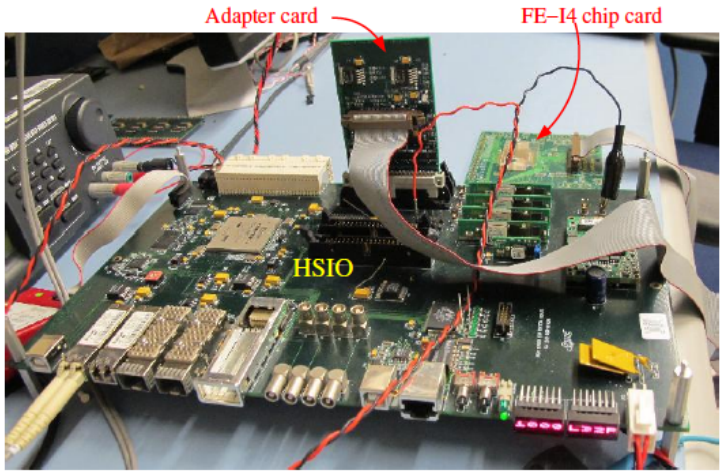
Development/Test
Machines
2x 1GE NIC

2x Dual-3GHz Xeon

Infrastructure
Server for
DHCP, DDNS
NFS, NTP

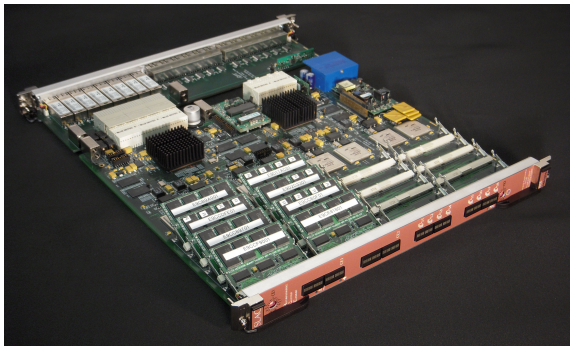
PowerEdge 2900

RCE applications to ATLAS pixel….and soon SCT



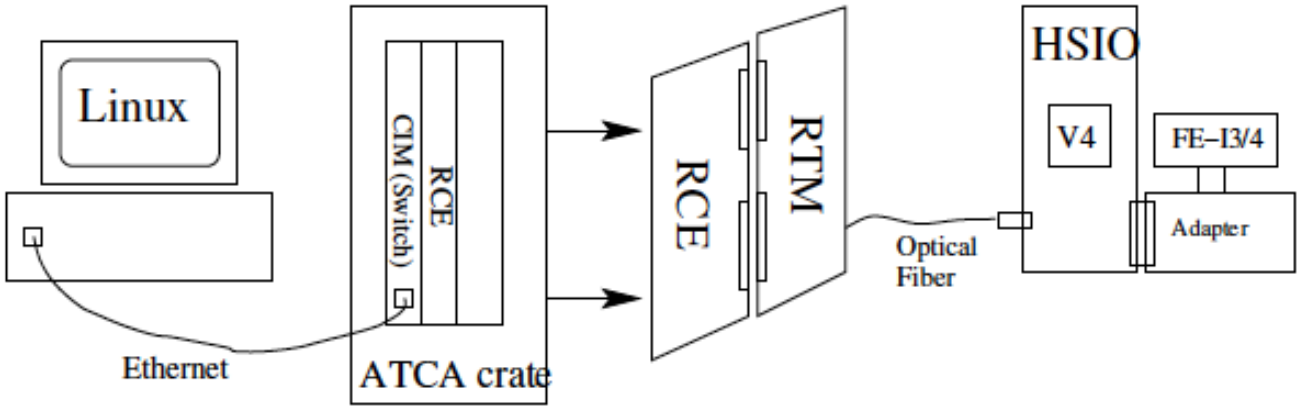
2-slot ATCA Shelf

- We're taking this existing technology and applying it to the phase-II upgrade of the ATLAS semiconductor tracker (SCT).
  - as yet untried!! We'll be the first group to do this.
  - "firmware" and software under development in context of current SCT DAQ setup
- We'll rewrite the current firmware and software being used in the pixel test setup
- Such systems will then be geared towards the high energy upgrade of ATLAS and LHC (phase-II in early 2020's)



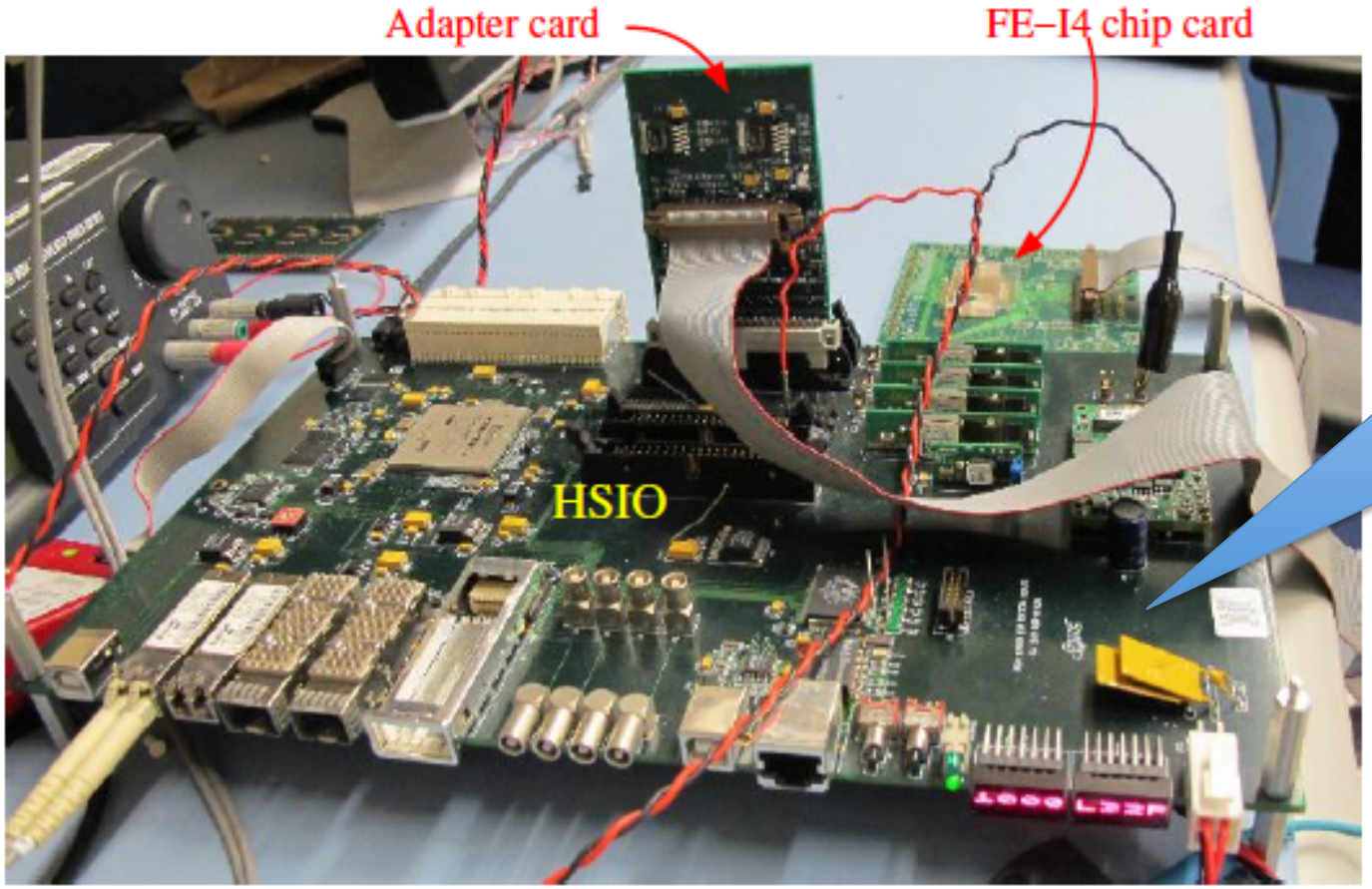
RCE/RTM

Our test stand setup



- The system is controlled from a Linux box.
- The RCE runs the calibration/DAQ software.
- An HSIO frontend interface board is connected through an optical fiber. The HSIO serializes the commands going to the pixel modules and deserializes the data coming from the pixel modules.
- There are different adapter boards:
  - Single channel adapter for the current ATLAS pixel frontend (FE-I3) modules.
  - Multi channel adapter for the current FE-I3 modules.
  - Single channel adapter for the next generation (FE-I4) chips.
  - A multi-channel adapter for 8 FE-I3 modules and 8 FE-I4 chips is in production.

HSIO board

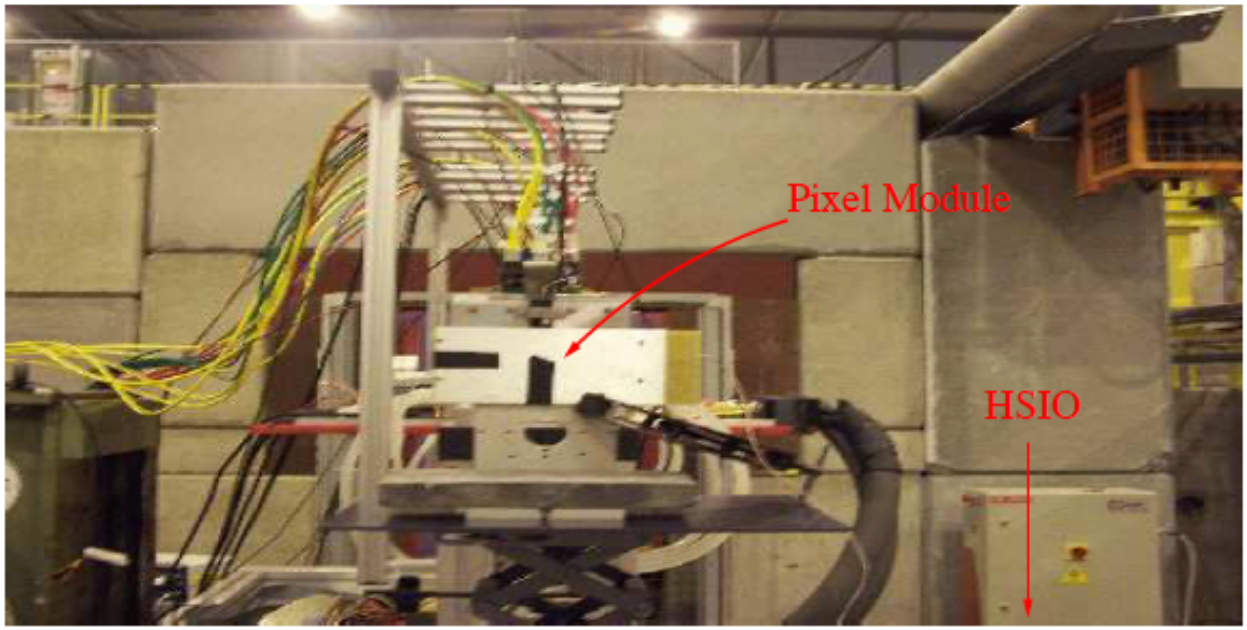


I moved to Adelaide earlier this year!!

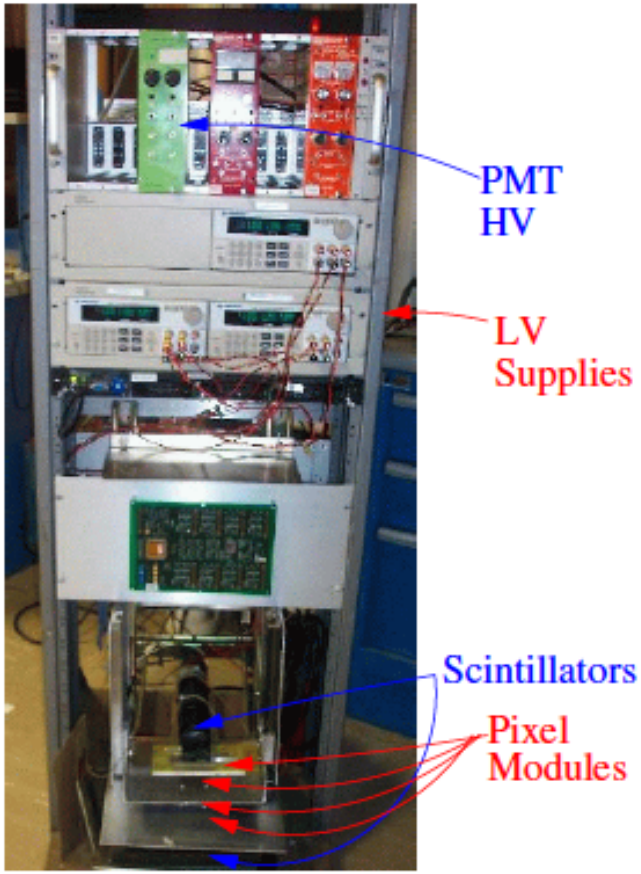
This board is the typical ROD replacement test board for the SCT upgrade.
This alone will be insufficient to readout the SCT for phase-II ATLAS (too slow)

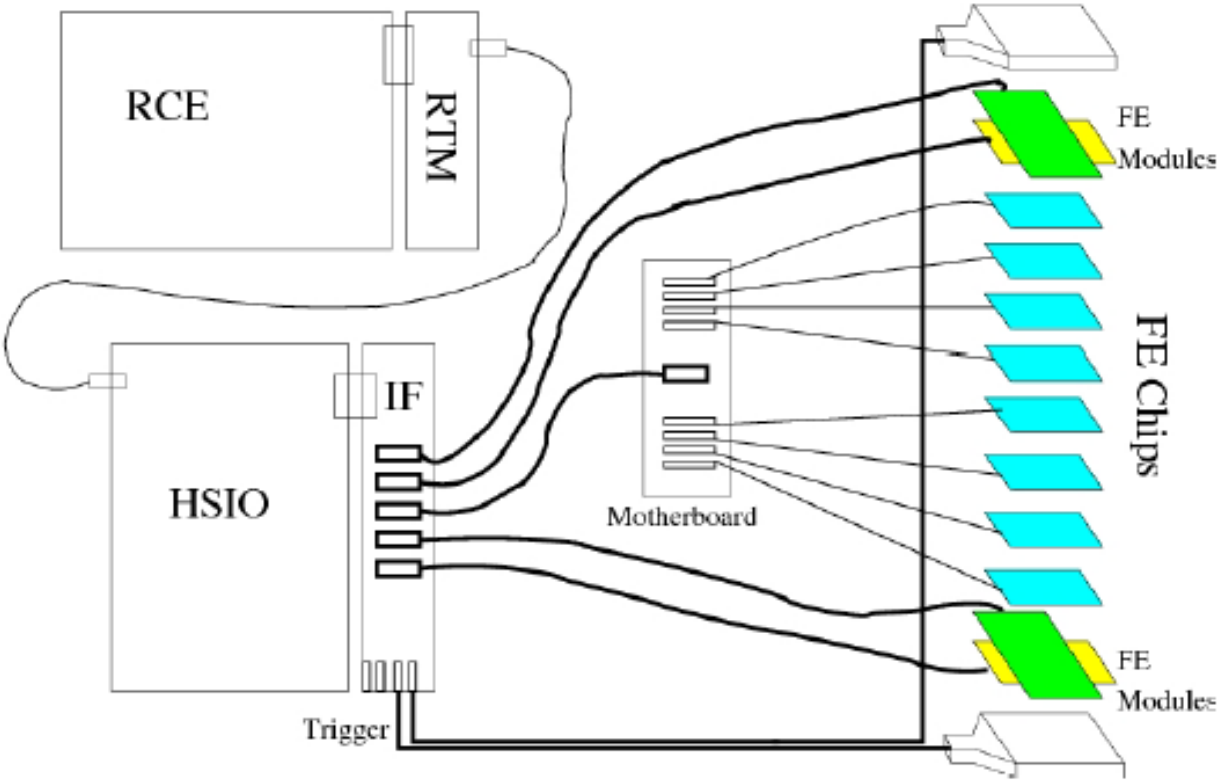
Test beam setup

- The RCE test setup can be used in a test beam.
- We ran the RCE in a 3-d test beam at CERN in June of 2010.
- Instantaneous trigger rates of ca. 500 Hz.
- With the new adapter board we will be able to run 8 FE-I4 chips simultaneously.



Cosmic Telescope!

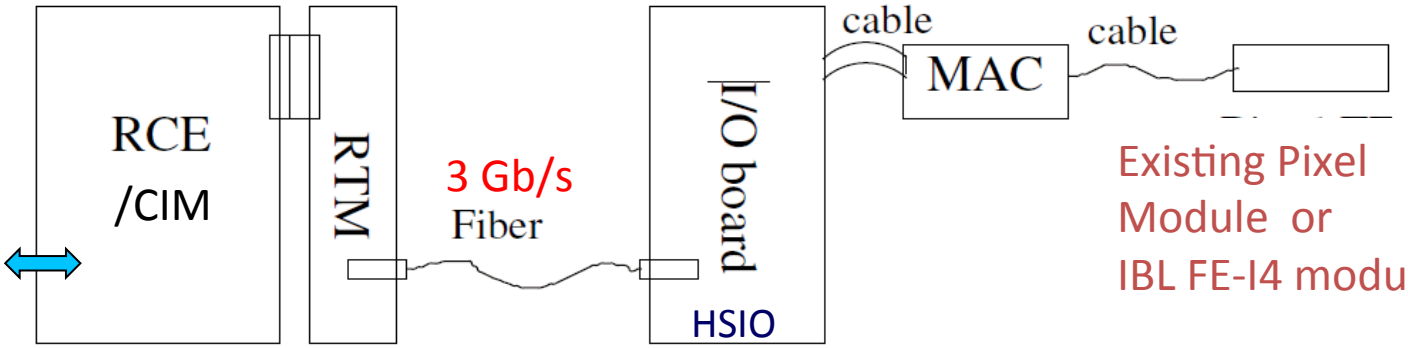




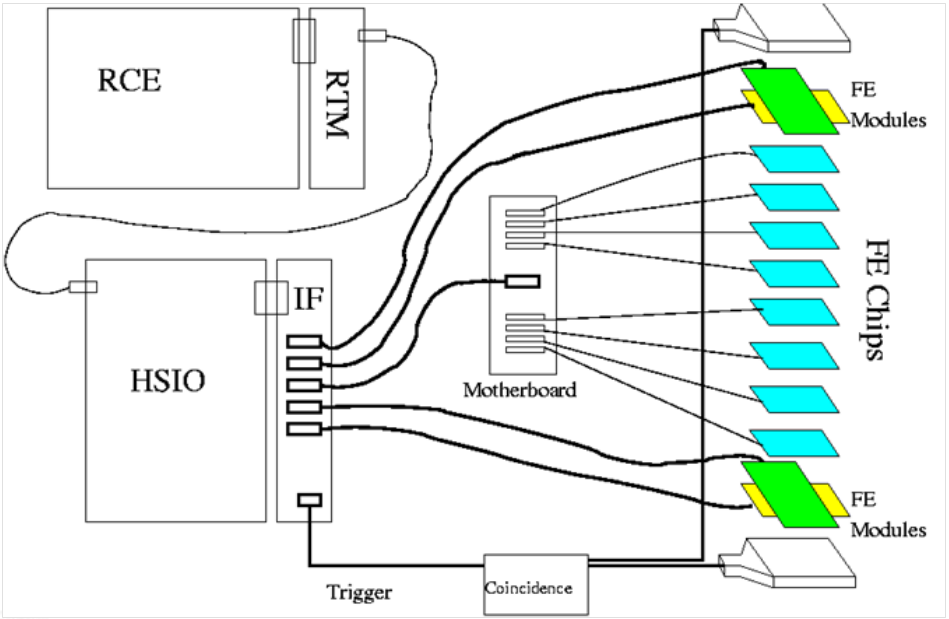
- Can be used for sensor testing in addition to test beam.
- Up to 4 scintillators for triggering, 4 pixel modules for tracking.
- Up to 8 single chip assemblies can be tested simultaneously.

Other pictures!!

Typical test stand



Cosmic Telescope @SLAC

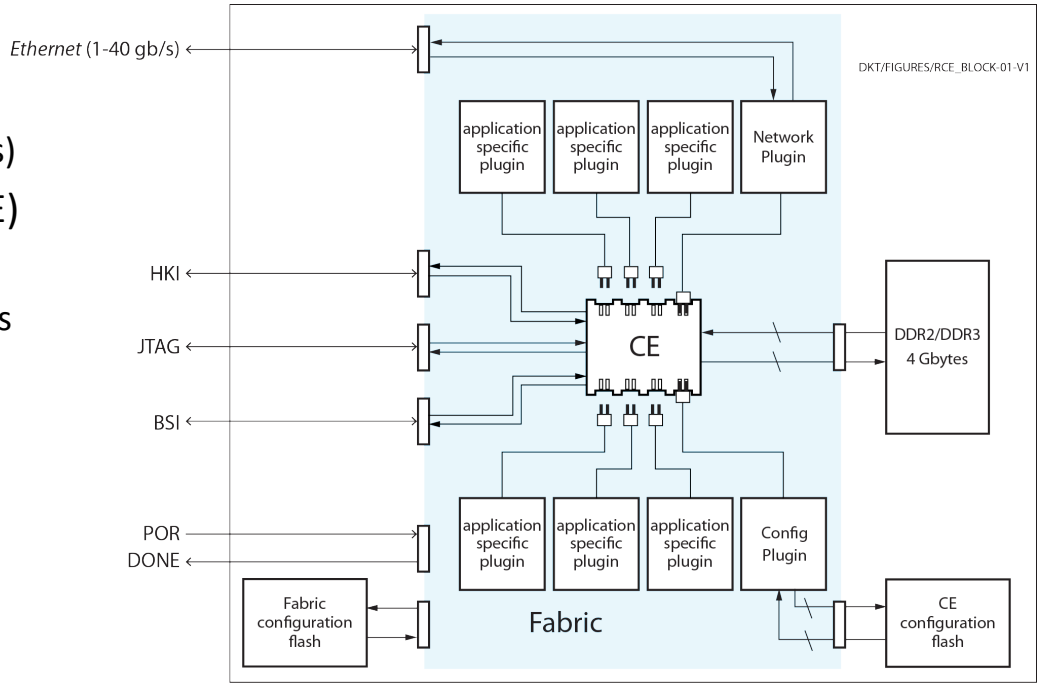


Other applications:

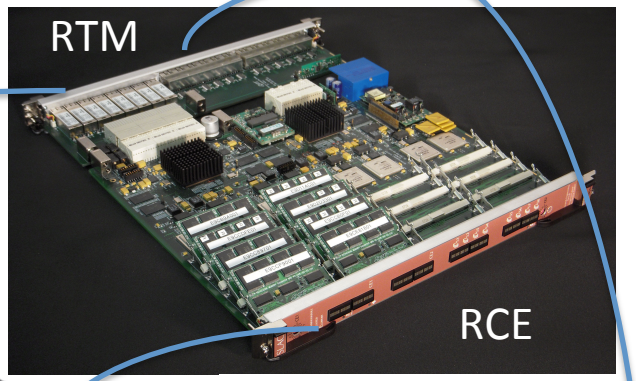
- Successful integration with EUDET @ CERN test beam.
- Preparation of IBL stave-0 (16 x FE-I4) readout/calibration tests for Jun/Jul 2011.

The RCE

- Based on SOC technology…
  - *Xilinx* Virtex-5 & ASP
- Has three principal components:
  - Programmable *Fabric*
    - Paired with configuration flash
    - Both soft & hard silicon (resources)
  - Programmable *Cluster-Element* (CE)
    - Paired with configuration flash
    - RAM (DDR2/DDR3), up to 4 Gbytes
  - *Plugins*
    - "Glues" fabric resources to CE
    - *Itself* is built from fabric resources
    - Comes bundled with two prebuilt:
      - Network (1-40 Gb/sec *Ethernet)*
      - Interface to CE flash
- CE has eight (8) sockets
  - 2 prewired to bundled plugins
  - 6 are application defined
- Two most "interesting", hardened resources:
  - DSP tiles (> 200 TeraMACS/Sec)
  - SerDes (+ support) (up to 12.5 Gbits/s)

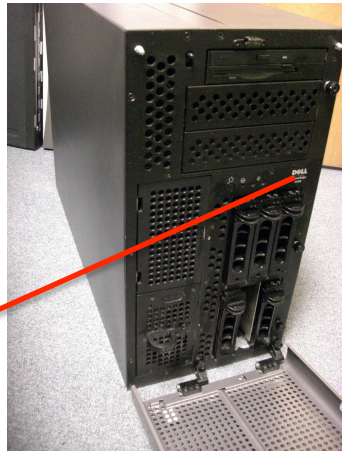


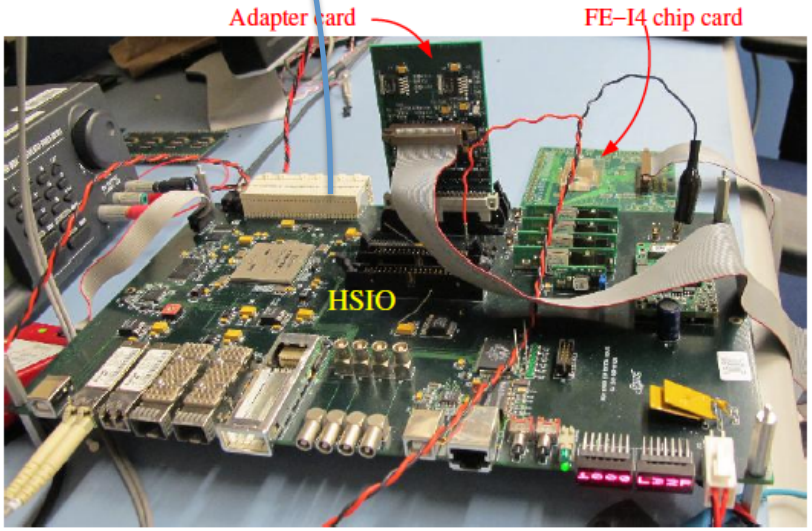
Pictorial view of our setup



ATCA Crate
w/ shelf manager
and power supply

ethernet



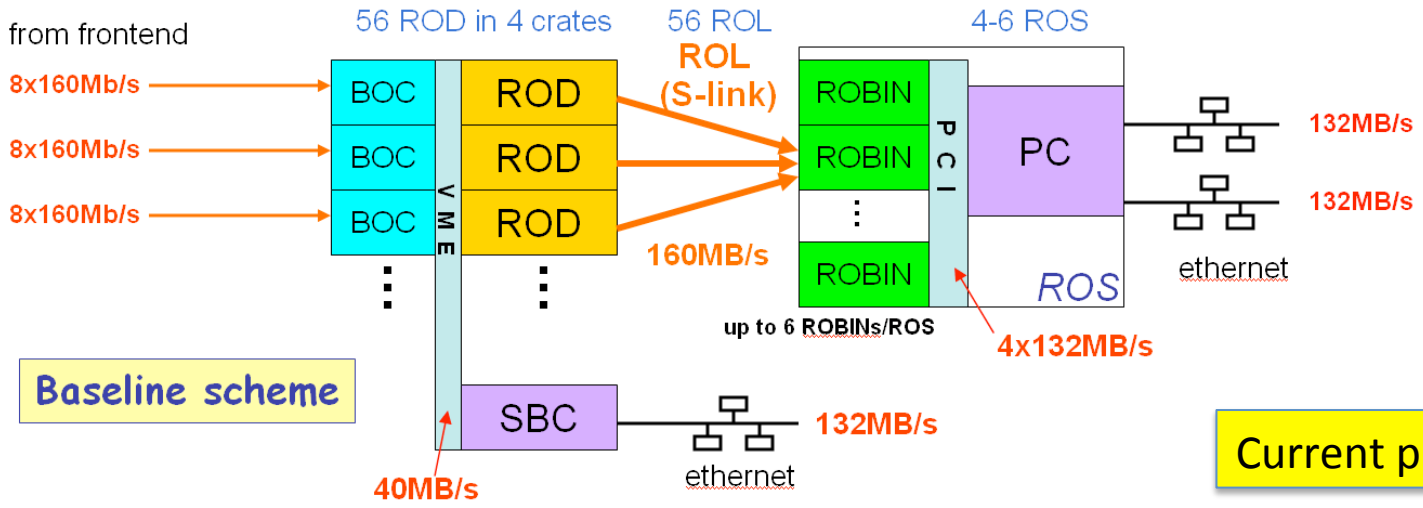


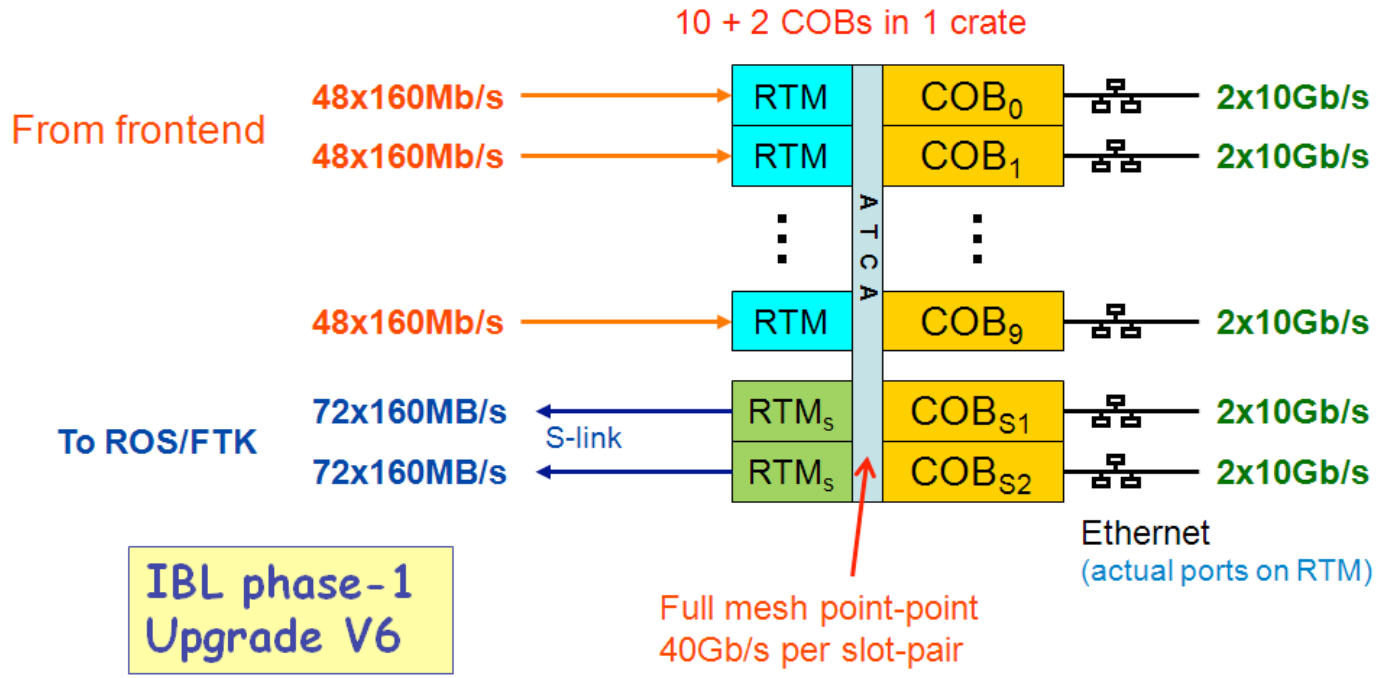
HSIO for continuity with previous systems
Reuse current DAQ framework of firmware

“Phase 2” Cluster on Board (COB)

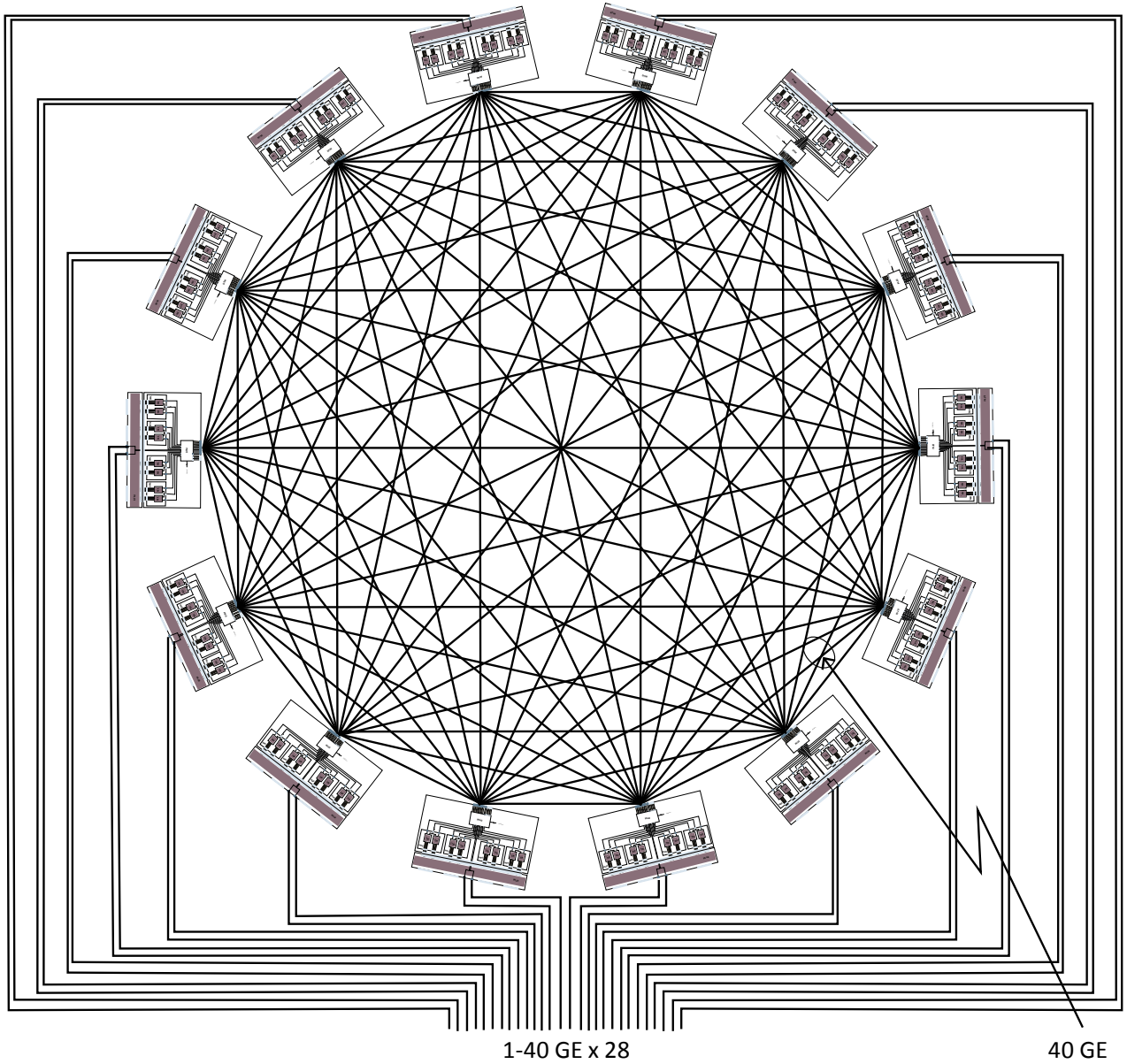
- “Mezzaninize” RCE & CI concepts
  - Decouples RCE & CI from ATCA (or any packaging standard)
- New ATCA Front-Board which supports:
  - The mezzanine concept
    - Decouples Front-Board from RCE & CI
  - The cluster concept
  - IPMI (shelf configuration & monitoring)
  - Full mesh backplanes
    - Applications require only a single type of board
    - Interoperability with any type of backplane
  - The ATCA for physics standard (PICMG 3.8)
  - Complete interoperability with any type of ATCA board
  - 10 Gbits/s signaling (both backplanes & Ethernet switching)
  - Generic, synchronous Timing & Trigger signal distribution

Comparison – Present and Future





Ethernet Topology of 14-slot ATCA shelf



Summary

- University of Adelaide High Energy Physicists are pursuing an upgrade solution to the ATLAS semiconductor tracker readout using ATCA/RCE based technologies
- The early phase technology has already proved it's worth in:
  - LCLS (Linear Coherent Light Source)
  - HPS (Heavy Photon Search)
  - ATLAS upgrade
- Future use of "phase 2" RCE system is underway for
  - LSST (Large Synoptic Survey Telescope) – The LSST camera of ~3 billion pixels needs to be read at rate of ~1Hz but each frame contains several Giga bytes of raw data.
  - LAr/TPC for LBNE (Long Baseline Neutrino Experiment)
  - PetaCache
- Stepping up to 40Gb ethernet readout will comfortably meet the need of future HL-LHC and others

Thank you for your attention!

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